REMARKS

The Final Office Action mailed May 3, 2005, has been received and reviewed. Claims 1 through 22 are currently pending in the application. Claims 1 through 22 stand rejected. Applicants propose to amend claims 1, 9, and 15, and respectfully request reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 112 Claim Rejections

Claims 1 through 22 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

The Office Action states:

> 3. Claims 1-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.
>
> The at least a second functional die ***formed and coupled as a unitary integral wafer segment*** with the first functional die (claim 1); the at least one nonfunctional die being ***formed on the unitary integral wafer segment*** (clams 6, 12 and 20); the two or more functional dice ***being on a unitary integral wafer segment*** (claim 9); and the first and second functional dice ***being on a unitary integral portion*** of the semiconductor wafer ***and*** further ***configured as an independently functional segment*** of the semiconductor wafer (fig. 15) are new subject matter. (Office Action, pp. 2-3; emphasis added).

Applicants respectfully disagree with the assertions that the amendments to the claims made in the prior Response to the Office Action do not comply with the written description requirement of 35 U.S.C. §112, first paragraph.

M.P.E.P. § 2173.05(e) provides:

> There is no requirement that the words in [a] claim must match those used in [a] specification disclosure. Applicants are given a great deal of latitude in how they choose to define their invention

> so long as the terms and phrases used define the invention with a reasonable degree of clarity and precision.

Furthermore, in *Staehelin v. Secher*, the Board held that "[s]atisfaction of the 'written description' requirement does not require an *haec verba* antecedence in the originally filed application." (24 USPQ2d 1513, 1519 (B.P.A.I. 1992)). In *Ex parte Parks*, the Board further elaborated:

> Adequate description under the first paragraph of 35 U.S.C. 112 does not require *literal* support for the claimed invention. . . . Rather, it is sufficient if the [] disclosure would have conveyed to one having ordinary skill in the art that an appellant had possession of the concept of what is claimed. (30 USPQ2d 1234, 1236 (B.P.A.I. 1994).

Applicants respectfully direct the Examiner's attention to several passages within Applicants' application as originally filed, which provide an adequate basis for the language at issue. Specifically, Applicants' as-filed application includes the following passages in support of the exemplary claim languages of "at least a second functional die ***formed and coupled as a unitary integral wafer segment*** with the first function die":

> Paragraph [0005]: The functional die group, once interconnected, is then ***segmented*** from the wafer while ***maintaining*** the ***unitary structural integrity*** of the functional die group . . ..
>
> Paragraph [0034]: The plurality of functional dice are ***integral in form*** and are ***not individually segmented*** as in the case of prior art applications but comprise a ***single contiguous*** semiconductor ***substrate*** . . ..
>
> Paragraph [0037]: Following the coupling together of functional die groups 106 and 108, the entire five-***die assembly may then be unitarily segmented from the wafer*** as a semiconductor device . . ..
>
> Abstract of the Disclosure: The functional die group, once interconnected, is then ***segmented*** from the wafer ***while maintaining the unitary integrity*** of the functional die group . . ..

From Applicants' written description in Applicants' as-filed patent application, it is apparent that Applicants, at the time of invention, were in possession of the exemplary concept of "at least a second functional die ***formed and coupled as a unitary integral wafer segment*** with the first function die" as illustrated by the various claim language at issue. Applicants also assert

that the as-filed patent application also provides written description support for Applicants' presently amended claim language:

> "the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die" (Applicants' Amended Independent Claim 1);
> "the two or more functional dice formed and maintained as a unitary integral wafer segment" (Applicants' Amended Independent Claim 9);
> "the first functional die and the second functional die formed and maintained as a unitary integral independently functional segment of the semiconductor wafer" (Applicants' Amended Independent Claim 15).

Accordingly, it is respectfully submitted that claims 1 through 22 comply with the written description requirement of 35 U.S.C. § 112, first paragraph, and requested that the 35 U.S.C. § 112, first paragraph, rejection of these claims be withdrawn.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,486,005 to Kim

Claims 1 through 4, 9, 11 and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kim (U.S. Patent No. 6,486,005). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Kim references does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of presently amended independent claims 1 and 9, and claims 2-4, 9, 11 and 13 depending therefrom, because the Kim reference does not describe, either expressly or inherently, the identical inventions in as complete detail as are contained in the claims.

Amended Independent Claim 1

The Office Action alleges:

> Kim discloses a semiconductor device comprising:
> a first functional die 31a including at least a first bond pad 32;
> at least a second functional die 31b including at least a second bond pad 32; and
> an adjacent die interconnection circuit 38 operably coupling the at least the first bond pad of the first functional die with the at least the second bond pad of the at least the second functional die (fig. 3G, column 3, lines 47 et seq.). (Office Action, p. 3).

Applicants respectfully disagree that the Kim reference anticipates Applicants' invention as claimed in amended independent claim 1 which reads:

> 1. A semiconductor device, comprising:
> a first functional die including at least a first bond pad;
> at least a second functional die including at least a second bond pad, ***the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die***; and
> an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die. (Emphasis added.)

In contrast, the Kim reference discloses:

> A fan-out type chip size package is efficiently fabricated at a level of wafer sized and stress buffer layers are formed at sides of the chip to rearrange bonding pads. (col. 3, lines 13-16)
> a first stress buffer layer 36 is formed at both sides of a unit semiconductor chip 31a, (col. 3, lines 19-20)
> the bonding pads 32 are formed on the upper part of the wafer 31 . . . [with] a first adhesive tape 33 . . . attached on the back of the wafer 31, . . . the scribe lane on the wafer 31 is then cut . . . to form unit semiconductor chips 31a and 31b. (col. 3, lines 48-56).
> Then, . . . the first adhesive tape 33 is expanded . . . [to] make the gap of the first cutting section 35 broaden . . . [then] a first stress buffer layer 36 is deposited on the whole surface including the first cutting section 35 . . . so that the semiconductor chips 31a and 31b are laterally supported. A material such as a silicon based benzocyclobutene (BCB), an oxide film or a nitride film is used as the first stress buffer layer 36, which acts as a buffer between chips and provides support. (col. 3, lines 57-67).

Clearly, the Kim reference discloses semiconductor chips individually formed on a wafer which are then individually separated from each other while attached to tape which can be

stretched to expand the overall footprint of the wafer by increasing the spacing between each of the individually sectioned semiconductor chips. The spaces between the chips are then filled with material that in essence "glues the further-spaced apart chips back together for a lead forming process where the leads are formed on the newly deposited "stress buffer layer" deposited between the individual chips. The chips are then individually cut from each other by scribing them in the "glued" regions.

Nothing in Kim discloses integrated circuits including "***the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die***" as claimed by Applicants. Specifically, Kim does not disclose "A semiconductor device, comprising: a first functional die including at least a first bond pad; at least a second functional die including at least a second bond pad, ***the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die***; and an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die" as claimed in Applicants' amended independent claim 1.

Therefore, independent claim 1, and claims 2-4 depending therefrom, are not anticipated by the Kim reference under 35 U.S.C. § 102. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

Amended Independent Claim 9

The Office Action alleges:

> Regarding claim 9, Kim discloses a segment of a semiconductor wafer, comprising: two functional dice 31a and 31b each including at least one bond pad 32; and an adjacent die interconnection circuit 38 for mutually operably coupling each at least one bond pad of the two functional dice to at least one other bond pad 32 of the two functional dice (fig. 3G, column 3, lines 47 et seq.). (Office Action, p. 4).

Applicants respectfully disagree that the Kim reference anticipates Applicants' invention as claimed in amended independent claim 9 which reads:

> 9. A segment of a semiconductor wafer, comprising:

> two or more functional dice each including at least one bond pad, ***the two or more functional dice formed and maintained as a unitary integral wafer segment***; and
> an adjacent die interconnection circuit for mutually operably coupling each at least one bond pad of the two or more functional dice to at least one other bond pad of the two or more functional dice. (Emphasis added.)

Applicants herein sustain the characterization of the description of Kim and arguments proffered above with reference to the lack of description regarding Applicants' invention as claimed. Specifically, Kim does not disclose "the two or more functional dice formed and maintained as a unitary integral wafer segment" as claimed by Applicants in amended independent claim 9.

Therefore, independent claim 9, and claims 11 and 13 depending therefrom, are not anticipated by the Kim reference under 35 U.S.C. § 102. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,486,005 to Kim in view of U.S. Patent No. 6,744,067 to Farnworth et al.

Claims 5, 10, 14 through 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Patent No. 6,486,005) in view of Farnworth et al. (U.S. Patent No. 6,744,067). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 5, 10, and 14 through 19 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Claim 5

Regarding claim 5, which depends from amended independent claim 1, Applicants sustain the above-proffered arguments that Kim does not teach, disclose or motivate Applicants' invention as claimed in amended independent claim 1. The Office Action introduces the Farnworth reference and alleges:

> Farnworth et al. disclose that a first functional die and a second functional die are separated by at least one nonfunctional die (column 3, lines 28-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to test the device structure of Kim by having the nonfunctional die between the first and second functional dice, as taught by Farnworth et al., for testing of each individual die or groups of dice in order to determine and segregate operation dice from non functional die (column 8, lines 25-28). (Office Action , p. 5)

A closer reading of Farnworth states that discloses "semiconductor die is fabricated according to conventional fabrication processes with each die including a defined number of die contacts that are electrically exposed for subsequent interconnection with other electronic components. One embodiment of the [Farnworth] invention contemplates busing contacts of interest together from at least one die to at least one other die for wafer-level testing." (Col. 2, lines 30-37).

Applicants respectfully submit that neither the Kim reference or the Farnworth reference, either individually or in any proper combination, teach, disclose or motivate Applicants' invention as claimed in independent claim 1 from which claim 5 depends, namely:

> 1. A semiconductor device, comprising:
> a first functional die including at least a first bond pad;
> at least a second functional die including at least a second bond pad, ***the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die***; and
> an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at

least a second functional die. (Emphasis added.)

Therefore, Applicants respectfully request that the rejection of dependent claim 5 be withdrawn.

Claims 10 and 14

Regarding claims 10 and 14, which depend from amended independent claim 9, Applicants sustain the above-proffered arguments regarding the Kim and Farnworth references and the respective lack of teaching, disclosure and motivation of Applicants' invention as claimed in amended independent claim 9.

Applicants respectfully submit that neither the Kim reference or the Farnworth reference, either individually or in any proper combination, teach, disclose or motivate Applicants' invention as claimed in independent claim 9 from which claims 10 and 14 depend, namely:

> 9. A segment of a semiconductor wafer, comprising:
> two or more functional dice each including at least one bond pad, ***the two or more functional dice formed and maintained as a unitary integral wafer segment***; and
> an adjacent die interconnection circuit for mutually operably coupling each at least one bond pad of the two or more functional dice to at least one other bond pad of the two or more functional dice. (Emphasis added.)

Therefore, Applicants respectfully request that the rejection of dependent claims 10 and 14 be withdrawn.

Claims 15 through 19

Regarding amended independent claim 15 and claims 16 through 19 which depend therefrom, Applicants sustain the above-proffered arguments regarding the Kim and Farnworth references and the respective lack of teaching, disclosure and motivation of Applicants' invention as claimed in amended independent claim 15.

Applicants respectfully submit that neither the Kim reference or the Farnworth reference, either individually or in any proper combination, teach, disclose or motivate Applicants' invention as claimed in amended independent claim 15 from which claims 16 through 19 depend, namely:

15. A semiconductor wafer, comprising:
a plurality of dice each including a bond pad, the plurality of dice segregated according to functional dice and nonfunctional dice; and
an adjacent die interconnection circuit operably coupling a first bond pad of a first functional die with a second bond pad of a second functional die, ***the first functional die and the second functional die formed and maintained as a unitary integral independently functional segment of the semiconductor wafer.*** (Emphasis added.)

Applicants herein sustain the above-recited arguments regarding the lack of teaching or suggestion of Kim and Farnworth, either individually or in any proper combination. Therefore, Applicants respectfully request that the rejection of amended independent claim 15, and claims 16 through 19 depending therefrom, be withdrawn.

Presumed Objections to Claims 6-8, 12 and 20-22/Allowable Subject Matter

Claims 6 through 8, 12, and 20 through 22 are presumed as remaining objected to as being dependent upon rejected base claims, but contain allowable subject matter and would be allowable if placed in appropriate independent form.

Applicants have amended the respective independent claims from which the presumed objected-to dependent claims depend. Applicants respectfully maintain that the presumed objected-to claims remain allowable in view of the amended independent claims.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 9, and 15 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1-22 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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